What is claimed is:

1. (Canceled) A vertical nano-transistor
with a source region (S),
with a drain region (D),
with a gate region (G) and
with a semiconductor channel region (3) between the source region (S) and the drain region (D),
the gate region (G) being formed by a metal film (1) in which the transistor is embedded such that the gate region (G) and the semiconductor channel region (3) form a coaxial structure and the source region (S), the semiconductor channel region (3) and the drain region (D) are arranged in a vertical direction and
the gate region (G) is provided with an electrical insulation (2) against the source region (S), the drain region (D) and the semiconductor channel region (3).

2. (Currently amended) The transistor of claim 23,
in which the semiconductor channel region is structured cylindrically.

3. (Currently amended) The transistor of claim 23,
in which the thickness of the metal film forming the vertical gate region is less than 100 µm, preferably 5 to 20 µm.

4. (Currently amended) The transistor of claim 23,
in which the diameter of the semiconductor channel region is several ten to several hundred nanometers.

5. (Currently amended) The transistor of claim 23,
in which the thickness of the electrical insulation between the gate region and the semiconductor channel is several ten to several hundred nanometers.

6. (Currently amended) The transistor of claim 23,
in which the thickness of the insulation layer on the upper and lower surface of the metal film is several micrometers.

7. (Currently amended) The transistor of claim 23,
wherein the semiconductor channel comprises a material selected from the group consisting of CuSCN, TiO_2, PbS, ZnO and another compound semiconductor.

8. (Currently amended) The transistor of claim 23,
wherein the source and the drain regions comprise a material selected from the group consisting of Au, Ag, Cu, Ni and Al.

9. (Currently amended) The transistor of claim 23,
wherein the source and the drain region are structured as dots.

10. (Currently amended) A memory arrangement, comprising:
a metal film;
a plurality of vertical nano-transistors according to claim 23 is arranged adjacent each other in the metal film.

11. (Currently amended) A method of fabricating vertical nano-transistors according to claim 1, including at least the following method steps

- forming holes in a thin metal film constituting the gate region of the transistor, for forming the channel region,
- applying insulation material to the walls of the holes,
- applying insulation material to the upper and lower surface of the metal film,
- applying semiconductor material in the insulated holes for forming the semiconductor channel region,
- applying contacts for forming the source and drain regions.

12. (Currently amended) The method of claim 11,
wherein the holes in the metal film are formed by focused ion beams.

13. (Currently amended) The method of claim 11,
wherein the holes in the metal film are formed by a laser beam.

14. (Currently amended) The method of claim 11,
wherein the insulation material is applied to the upper and lower surface of the metal film by thin-film technology.

15. (Currently amended) The method of claim 11,
wherein the insulation material is applied to the wall of the holes and to the upper and lower surface of the metal film by vacuum filtration of a polymer solution.

16. (Currently amended) The method of claim 11,
wherein the insulation material is applied to the wall of the holes and to the upper and lower surface of the metal foil by electro-chemical deposition.

17. (Currently amended) The method of claim 11,
wherein the insulation material is applied to the wall of the holes and to the upper and lower surface of the metal foil by chemical deposition.

18. (Currently amended) The method of claim 11,
wherein the semiconductor channel region comprises a material selected from the group consisting of CuSCN, TiO_2, PbS, ZnO and another compound semiconductor.

19. (Currently amended) The method of claim 11,
wherein the semiconductor material is introduced into the insulated holes by electro-chemical bath precipitation.

20. (Currently amended) The method of claim 11, wherein the semiconductor material is introduced into the insulated holes by chemical deposition.

21. (Currently amended) The method of claim 11, wherein the semiconductor material is introduced into the insulated holes by the ILGAR process.

22. (Currently amended) The method of claim 11, wherein the source and drain regions comprise a material selected from the group consisting of Au, Ag, Cu, Ni and Al.

Add the following new claim:

23. (New) A vertical nano-transistor, comprising:

a source region;

a drain region;

a semiconductor channel region intermediate the source region and the drain region;

a gate region comprising a metal film, the transistor being embedded in the metal film such that the gate region and the semiconductor channel region form a coaxial structure and the source region, the semiconductor channel region and the drain region being vertically arranged; and

the gate region being electrically insulated from the source region, the drain region and the semiconductor channel region.